REMARKS

The present Amendment is filed in response to the Examiner's Office Action mailed September 25, 2002. Claims 1-31 were pending. Claims 11-21 and 26-31 were withdrawn from consideration. Claims 1, 22, and 24 are amended. Claims 1-10 and 22-25 are now pending in view of the above amendments.

Reconsideration of the application is respectfully requested in view of the following remarks. For the Examiner's convenience and reference, Applicant's remarks are presented in the order in which the corresponding issues were raised in the Office Action.

A. Rejection Under 35 U.S.C. § 112

The Examiner rejects claims 1-10 and 24 under 35 U.S.C. § 112, ¶ 2, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. In particular, the Examiner rejects independent claims 1 and 24 for including claim limitations that lack sufficient antecedent basis. In response, Applicant has amended each of these claims in the following manner:

In independent claim 1: "Said gate oxide coating" has been amended to read "said gate oxide *layer*."

In dependent claim 24: The claim limitation "said conducting polysilicon layer" has been changed to read "said *upper* polysilicon layer".

Applicant submits that the above claim amendments add no new subject matter. Further, Applicant submits that these amendments eliminate any basis for rejection of the present claims alleged by the Examiner. Applicant therefore respectfully requests that the rejection of claims 1-10 and 24 under Section 112, Paragraph 2, be removed and that these claims be allowed.

B. **Claim Rejection Under 35 U.S.C. § 102**

In the Office Action, the Examiner rejects claims 1 and 6-8 under 35 U.S.C. § 102(b) as being anticipated by, or in the alternative, under 35 U.S.C. § 103(a), as being obvious over United States Patent No, 5,708,284 to *Onishi*. As will be shown however, *Onishi* fails to teach each and every element of the pending claims, and thus is neither an anticipatory reference nor renders the present invention obvious.

Onishi discloses a non-volatile random access memory cell for use in electronic applications. In particular, *Onishi* teaches a a metal-ferroelectric-semiconductor ("MFS") memory cell comprising a MFS transistor disposed atop a semiconductor substrate 1, the substrate having a plurality of impurity diffusion layers disposed therein. The MFS transistor includes a bottom gate electrode 5b that directly connects through a hole formed in a gate insulation film 2 to a first impurity diffusion layer 6a. A bottom electrode 8 is disposed atop the bottom gate electrode. A ferroelectric film 9 and top electrode 10 are disposed in a stacked configuration atop the bottom electrode. A metal-oxide-semiconductor ("MOS") transistor is also included adjacent the MFS transistor and comprises a gate insulation film 2 and a gate electrode 5a. *See Onishi*, Figure 1; column 7, line 60- column 8, line 34.

The claimed invention is substantially different than the device taught by *Onishi*. Specifically, independent claim 1 requires the presence of a single transistor ferroelectric memory cell including a semiconductor substrate having source, drain, and channel regions, and "a gate oxide layer disposed on said semiconductor substrate to cover *the entirety of* said drain, channel, and source regions." *Onishi* teaches no such structure. Indeed, in contrast to the present invention, *Onishi* teaches a gate insulation film that specifically *does not* cover the

entirety of the impurity diffusion layers that serve source and drain regions for the memory cell of *Onishi*. This is clearly shown in column 7 of *Onishi*, lines 62-65, which state:

> First, as shown in FIG. 4, the gate insulation film 2 is formed on the entire surface of the P-type silicon substrate 1. Then, *a contact hole 4 is formed in a desired region of the gate insulation film 2* by using a resist mask 3. (Emphasis added.)

The gate insulation film 2 is left bare over the impurity diffusion layer 6a (See Figure 1) in order to produce a direct ohmic contact between the impurity diffusion layer and the bottom gate electrode 5b via contact hole 4 as seen in column 7, lines 35-39, which state:

> The MFS transistor includes, as well as the impurity diffusion layer 6a shared with the MOS transistor, a bottom gate electrode 5b having a *direct connection* C with a portion of the impurity diffusion layer 6a . . . . (Emphasis added.)

The absence of the gate insulation film over the impurity diffusion layer, thereby facilitating direct contact of the bottom gate electrode with the impurity diffusion layer, is done so as to allow a sufficient amount of voltage to be provided to the ferroelectric portion of the MFS transistor, thereby significantly reducing current consumption. *See Onishi*, column 10, lines 57-64. Thus, not only does *Onishi* fail to teach a gate oxide layer covering the entirety of the drain channel and source regions of a ferroelectric memory cell, but it teaches away from such a layer so as to allow direct contact between select memory cell components. *Onishi* is therefore inapposite to the present claimed invention. Accordingly, Applicant submits that *Onishi* fails to teach or suggest each and every element of independent claim 1, and therefore respectfully requests that rejection of the claim under Section 102 and/or Section 103 be removed. Moreover, inasmuch as claims 2-10 are dependent on independent claim 1, Applicant submits that these claims are also allowable for at least the reasons given above.

The Examiner also rejects claims 22-25 under 35 U.S.C. § 102(b) as being anticipated by PCT Application No. WO 00/28596 to Schlosser *et al.* ("*Schlosser*"). However *Schlosser* also fails to teach or suggest each and every element of the claims, and thus is not an anticipatory reference.

Schlosser generally discloses a memory cell arrangement comprising a selection transistor, a memory transistor, and a ferroelectric capacitor. In particular, *Schlosser* appears to teach, in Figure 2, a substrate ("Halbleitersubstrat") 1 having source/drain regions ("Source-/Drain-Gebiet") 2, 3, and 4 disposed therein. A ferroelectric memory structure is disposed on the substrate and comprises a gate oxide ("Gateoxid") 5, a control electrode GS, a barrier layer ("Barriereschicht") 6, and a ferroelectric structure comprising bottom and top electrodes ("Kondensatorelektrode") KE1 and KE2 disposed on either side of a ferroelectric layer ("ferroelektrische schicht") FS.

The present invention is patentably distinct from the device taught by *Schlosser.* In particular, amended claim 22 requires the presence of a ferroelectric memory cell having a semiconductor substrate including a drain, a source, and a channel, and further including "a gate oxide *substantially covering the drain, source, and channel.*" Nowhere does *Schlosser* teach such a structure. Though *Schlosser* does include a gate oxide 5 in its memory cell structure, this gate oxide does not substantially cover the drain, source, and channel. Indeed, neither of the source/drain regions 3 nor 4 is covered at all by the gate oxide 5, and the source/drain region 2 is only slightly covered thereby. Consequently, *Schlosser* fails to teach or suggest each and every element of amended independent claim 22, or claims 23-25 that depend therefrom. Applicant therefore respectfully requests that rejection of these claims under Section 102 be removed.

C. **Claim Rejections under 35 U.S.C. § 103**

The Examiner rejects claim 1 under 35 U.S.C. § 103(a) as being unpatentable over *Schlosser* in view of United States Patent No. 5,798,548 to *Fujiwara* and United States Patent No. 5,959,879 to *Koo*. However, as will be shown, *Schlosser*, either alone or in combination with *Fujiwara* and *Koo*, does not teach or obviously suggest each and every element of the pending claims and thus does not make obvious the present invention.

The teachings of *Schlosser* are discussed above. Applicant submits that independent claim 1 is substantially different from the device taught by *Schlosser*. In particular, independent claim 1 requires the presence of "a gate oxide layer disposed on said semiconductor substrate to cover the entirety of said drain, channel, and source regions." As already discussed, *Schlosser*, among other differences, fails to teach such a layer. At best, Figure 2 shows the gate oxide 5 of *Schlosser* merely adjacent to, but not covering, any of the source/drain regions 2, 3, or 4. *Schlosser* is therefore inapplicable to the present claims rejected under Section 103, and thus the Examiner has failed to make out a *prima facie* case of obviousness. Applicant therefore respectfully submits that claim 1, as well as claims 2-10 depending therefrom, are allowable.

Applicant further submits that *Schlosser* differs from the present invention in other respects as well. Particularly, amended independent claim 1 requires the presence of "an upper conductive layer disposed on said ferroelectric gate unit *and a portion of said gate oxide layer* such that said upper conductive layer and said top electrode of said ferroelectric gate unit are in electrical communication." *Schlosser* fails to teach this structure as well. Indeed, though *Schlosser* teaches a conducting junction line ("leitende Verbindung") 11 atop both the source/drain region 3 and the top electrode KE2, this junction line is not disposed on or anywhere near a portion of the gate oxide 5. *Fujiwara* and *Koo* also fail to teach the structure

required in claim 1. Thus, for this reason as well, *Schlosser* fails to teach or suggest all of the limitations of claim 1. Applicant therefore respectfully submits that claims 1-10 are allowable and that the above rejection under Section 103 should be withdrawn.

The Examiner rejects additional claims under 35 U.S.C. § 103(a). In particular, the Examiner rejects claim 3 as being unpatentable over *Onishi* in view of United States Patent No. 6,294,807 B1 to Chittipeddi *et al.* and United States Patent No. 6,100,558 to Krivokapic *et al.* Claim 5 is rejected as being unpatentable over *Schlosser* in view of *Fujiwara* and *Koo* and further in view of the *Jaeger* reference. Claim 9 is rejected as being unpatentable over *Schlosser* in view of *Fujiwara* and *Koo*, and further in view of United States Patent No. 6,420,742 to Ahn *et al.* Claim 10 is rejected as being unpatentable over *Onishi* in view of United States Patent No. 6,172,392 B1 to Schmidt *et al.*

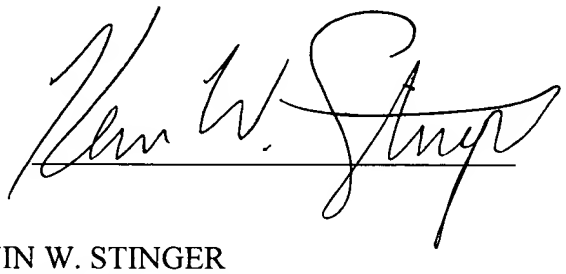
Applicant notes that each of the above rejections is partly based on either the *Onishi* or *Schlosser* reference. It is further noted that each of the rejected claims is dependent upon amended independent claim 1. As was previously discussed, the teachings of *Onishi* and *Schlosser* are inapplicable to the present invention as applied to claim 1 for failing to teach or suggest each of the limitations contained in that claim. Thus, *Onishi* and *Schlosser* are both equally inapplicable to the present claims rejected under Section 103 for at least the above reasons, that is, their failure to teach or suggest all of the claim limitations contained not only in independent claim 1, but also the limitations contained in the presently rejected dependent claims. Thus, the Examiner has failed to make out a *prima facie* case of obviousness. Applicant therefore respectfully submits that claims 3, 5, 9, and 10 are allowable and that the above rejection under Section 103 should be withdrawn.

CONCLUSION

In view of the discussion and amendments submitted herein, Applicant respectfully submits that each of the pending claims 1-10 and 22-25 is now in condition for allowance. Therefore, reconsideration of the rejection is requested and allowance of those claims is respectfully solicited. In the event that the Examiner finds any remaining impediment to a prompt allowance of this application that can be clarified in a telephonic interview, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Respectfully submitted,

Date: March 25, 2003

By: 

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